Code No: 137JD **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech IV Year I Semester Examinations, January/February - 2023

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.

ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.

iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions

PART – A

(25 Marks)

1.a)	List out different IC technologies including number of gates.	[2]
b)	When the channel is said to be pinched –off?	[3]
c)	Differentiate two scaling techniques.	[2]
d)	Draw the stick diagram of a 2 input NAND gate using CMOS.	[3]
e)	Define Fan – in.	[2]
f)	Draw the basic structure of a dynamic CMOS gate.	[3]
g)	Mention different clocking mechanisms.	[2]
h)	Compare SRAM, DRAM and ROM.	[3]
i)	Mention different FPGA logic families.	[2]
j)	Draw the typical architecture of PLA.	[3]

PART – B

(50 Marks)

2.a)	Draw and explain about BICMOS inverter.	
b)	What is latch –up? Explain the condition with remedial measures.	[5+5]
	OR	
3.a)	Explain the structures of nMOS enhancement mode, depletion mode and p-MOS enhancement mode transistors.	
b)	Explain the NMOS fabrication procedure.	[5+5]
4.a)	Explain about CMOS lambda based design rules with examples.	
b)	Draw stick diagram and layout diagram of CMOS inverter.	[5+5]
	OR	
5.	Design a stick diagram for two input nMOS NAND and NOR gates?	[10]

6.a) What is meant by sheet resistance R_S? Explain the concept of R_S applied to MOS ransistors.

b) Calculate the gate capacitance value of 5mm technology minimum size transistor with gate to channel value is 4×10^{-4} pF/mm^2. [5+5]

OR

7.a) How switch logic can be implemented using Pass Transistors? Explain.

b) Realize basic gates using NMOS. [5+5]

8.a) Describe the general considerations of subsystem design processes.

b) Discuss the clocked sequential circuits like counters and memories. [5+5]

OR

9.a) Explain the structured design approach of parity generator.

b) Explain the design of a 4-bit shifter. [5+5]

10.a) What are FPGAs? Explain the principle and operation.

b) Explain how the pass transistors are used to connect wire segments for the purpose of FPGA programming. [5+5]

OR

11. Discuss the need for testing, Test Principles and CMOS Testing. [10]

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